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(54) Read circuit for a nonvolatile memory

(57) The read circuit (1') comprises an array branch (6) having an input array node (22) connected, via an array bit line (8), to an array cell (10); a reference branch (12) having an input reference node (32) connected, via a reference bit line (14), to a reference cell (16); a current-to-voltage converter (18) connected to an output array node (56) of the array branch (6) and to an output reference node (58) of the reference branch (12) to supply on the output array node (56) and the output reference node (58) the respective electric potentials (V_M, V_R) correlated to the currents flowing in the array memory cell (10) and, respectively, in the reference memory cell (16); and a comparator (19) connected at input to the output array node (56) and output reference node (58) and supplying as output a signal (OUT) indicative of the contents stored in the array memory cell (10); and an array decoupling stage (80) arranged between the input array node (22) and the output array node (56) to decouple the electric potentials of the input and output array nodes (22, 56) from one another.

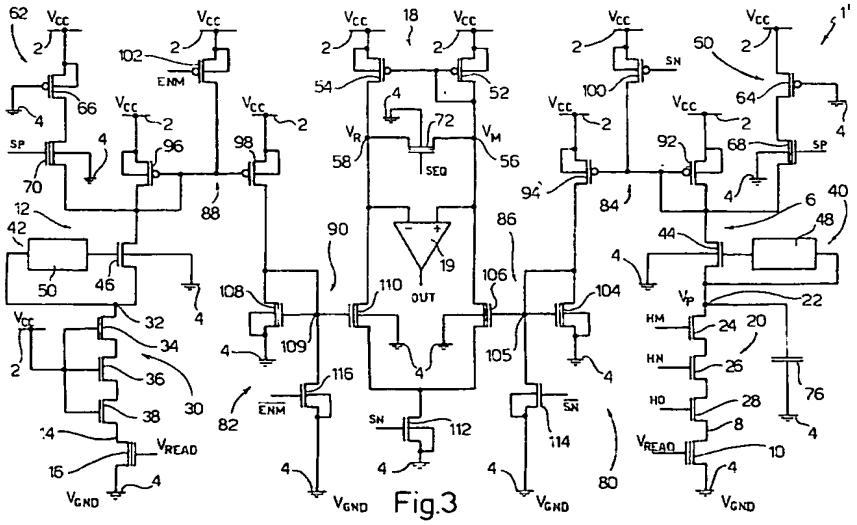

Fig.3

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Description

[0001] The present invention regards a read circuit for a nonvolatile memory.

[0002] As is known, in a floating gate nonvolatile memory cell, storage of a logic state is carried out by programming the threshold voltage of the cell itself through the definition of the quantity of electric charge stored in the floating gate region.

[0003] According to the information stored, memory cells may be distinguished into erased memory cells (logic state stored "1"), in which no electric charge is stored in the floating gate region, and written or programmed memory cells (logic state stored "0"), in which an electric charge is stored in the floating gate region that is sufficient to determine a sensible increase in the threshold voltage of the memory cell itself.

[0004] The most widespread method for reading nonvolatile memory cells envisages the comparison between a quantity correlated to the current flowing through the memory cell to be read and a similar quantity correlated to the current flowing through a memory cell having known contents.

[0005] In particular, to carry out reading of a memory cell, a read voltage is supplied to the gate terminal of the memory cell which has a value comprised between the threshold voltage of an erased memory cell and that of a written memory cell, in such a way that, if the memory cell is written, the read voltage is lower than the threshold voltage, and hence no current flows in the memory cell itself, whereas, if the memory cell is erased, the read voltage is higher than the threshold voltage, and hence current flows in the cell.

[0006] Reading of a memory cell is carried out by a read circuit known as "sense amplifier", which, in addition to recognizing the logic state stored in the memory cell, also provides for the correct biasing of the drain terminal of the memory cell.

[0007] A read circuit for a nonvolatile memory is, for example, described in the European Patent Application EP-A-0814480 filed on June 18, 1996 in the name of the present applicant.

[0008] According to what is illustrated in Figure 1, the sense amplifier, indicated as a whole by the reference number 1, comprises a supply line 2 set at the supply voltage V_{CC}; a ground line 4 set at the ground voltage V_{GND}; an array branch 6 connected, through an array bit line 8, to a nonvolatile array memory cell 10 the contents of which it is desired to read; a reference branch 12 connected, through a reference bit line 14, to a nonvolatile reference memory cell 16 the contents of which are known; a current-to-voltage converting stage 18 connected to the array branch 6 and reference branch 12 to convert the currents flowing in the array memory cell 10 and in the reference memory cell 16 into respective electric potentials; and a differential comparator stage 19 having the purpose of comparing these electric potentials and supplying at an output an output logic signal OUT indicative of the binary information "0" or "1" stored in the array memory cell 10.

[0009] In particular, the array cell 10 and reference cell 16 have drain terminals receiving the same read signal V_{READ}, drain terminals connected to the array bit line 8 and, respectively, to the reference bit line 14, and source terminals connected to the ground line 4.

[0010] The array branch 6 comprises an array column decoding block 20 connected between a node 22 (hereinafter indicated by the term "input array node 22") and the array bit line 8, and is made up of three NMOS transistors 24, 26, 28 connected in series and receiving on gate terminals respective column decoding signals HM, HN, HO, whilst the reference branch 12 comprises a reference column decoding block 30 connected between a node 32 (hereinafter indicated by the term "input reference node 32") and the reference bit line 14, and is formed of three NMOS transistors 34, 36, 38 connected in series, having gate terminals connected to the supply line 2 and having the purpose of setting the drain terminal of the reference memory cell 16 in the same load conditions as the drain terminal of the array memory cell 10.

[0011] The array branch 6 and the reference branch 12 comprise an array biasing stage 40 and, respectively, a reference biasing stage 42 having the purpose of biasing at a preset potential, typically 1 V, the input array node 22 and, respectively, the input reference node 32.

[0012] The array biasing stage 40 and the reference biasing stage 42 have an identical circuit structure and each comprise a fedback cascode structure formed of an NMOS transistor 44 and an NMOS transistor 46, respectively, and of a regulator 48 and a regulator 50, respectively. In particular, the NMOS transistors 44 and 46 have source terminals connected, on the one hand, to the input terminals of respective regulators 48 and 50, and, on the other, to the array bit line 8 and, respectively, to the reference bit line 14, drain terminals connected to the current-to-voltage converter stage 18, and gate terminals connected to the output terminals of the respective regulators 48, 50.

[0013] The current-to-voltage converter stage 18 consists of a current mirror having the purpose of carrying out the above mentioned current-to-voltage conversion and comprising a first diode-connected PMOS transistor 52 arranged on the array branch 6, and a second PMOS transistor 54 arranged on the reference branch 12. In particular, the PMOS transistors 52 and 54 have gate terminals connected together and to the drain terminal of the PMOS transistor 52, source and bulk terminals connected to the supply line 2, and drain terminals connected, respectively, to the drain terminal of the NMOS transistor 44 and the drain terminal of the NMOS transistor 46 and defining respective nodes 56, 58, hereinafter indicated by the term "output array node 56 and output reference node 58".

[0014] The array branch 6 and the reference branch 12 further comprise an array precharging stage 60 and,

respectively, a reference precharging stage 62, which have the purpose of precharging the output array node 56 and, respectively, the output reference node 58 through respective current paths arranged in parallel to the current path defined by the current-to-voltage converter stage 18.

[0015] In particular, the array precharging stage 60 and the reference precharging stage 62 are designed in such a way as to be able to supply, for the precharging of the output array node 56 and the output reference node 58, and hence of the parasitic capacitances associated to said nodes, a much larger current than the one which, on account of their reduced size, the PMOS transistors 52 and 54 of the current-to-voltage converter stage 18 are able to supply, so enabling the precharging phase of these nodes to be speeded up considerably.

[0016] In detail, the array precharging stage 60 and the reference precharging stage 62 present an identical circuit structure and each comprise a PMOS transistor 64 and, respectively, a PMOS transistor 66, and an NMOS transistor 68 and, respectively, an NMOS transistor 70, having high conductivity, that is, a high W/L ratio, connected in series and arranged between the supply line 2 and the output array node 56 and, respectively, between the supply line 2 and the output reference node 58.

[0017] In particular, the PMOS transistors 64 and 66 have source terminals and bulk terminals connected to the supply line 2, gate terminals connected to the ground line 4, and drain terminals connected to the drain terminal of the NMOS transistor 68 and, respectively, to the drain terminal of the NMOS transistor 70; the said NMOS transistors 68 and 70 in turn have gate terminals receiving one and the same precharging signal SP, bulk terminals connected to the ground line 4, and source terminals connected to the output array node 56 and, respectively, to the output reference node 58.

[0018] The comparator stage 19 has a non-inverting input terminal connected to the output array node 56 and an inverting input terminal connected to the output reference node 58, and supplies, on an output terminal, the output signal OUT.

[0019] Finally, the sense amplifier 1 comprises an equalization stage formed of an NMOS transistor 72 having drain terminal connected to the output reference node 58 and source terminal connected to the output array node 56, bulk terminal connected to the ground line 4, and gate terminal receiving an equalization signal SEQ having the purpose of issuing a command for turning on the NMOS transistor 72 only during the phase of equalization of the output array node 56 and the output reference node 58, in order to short-circuit the aforesaid nodes together to set them at one and the same equalization potential.

[0020] Also connected to the array bit line 8 is a plurality of array cells arranged on the same array column, the said cells being schematically represented in Figure 1 by an array equivalent capacitor 76, which, for convenience of description, is represented as being directly connected to the input array node 22, and the capacitance of which typically has values of 2-3 pF.

[0021] For a detailed description of the operation of the sense amplifier 1 and of the advantages that it makes possible, see the aforementioned patent application. Here it is emphasized that the main difference between the sense amplifier 1 described in the above mentioned patent application and the sense amplifiers according to the prior art lies in the fact that in the sense amplifier 1 described above it is the PMOS transistor 52, to which the array branch 6 is connected, that is diode-connected, whereas in the prior art the sense amplifier it is the PMOS transistor 54, to which the reference branch 12 is connected, that is diode-connected.

[0022] In the sense amplifier 1 it is therefore the current generated by the array memory cell 10 that is mirrored on the reference branch 12, i.e., multiplied by a mirror factor N, whereas, in the known art, it is the current generated by the reference memory cell 16 that is mirrored on the array branch 6, and this substantial difference enables reading of the array cells to be carried out also in the presence of low supply voltages without extending the read times as compared to the operating conditions in which the supply voltage is high.

[0023] With the amplification of the current flowing in the array memory cell 10, the use of the classic equalization network, which envisages the use of a transistor that turns on only during the precharging and equalization phases to short-circuit the output array node 56 and the output reference node 58, may no longer be sufficient when the aim is to obtain particularly reduced read times at low supply voltages.

[0024] In particular, unlike what occurs in the sense amplifiers according to the known art, the read times that can be obtained with the sense amplifier 1 described above at low supply voltages are markedly influenced by an erroneous definition of the equalization potential of the output array node 56.

[0025] In fact, if for example the equalization potential to which the output array node 56 is brought during the equalization phase is greater than a preset reference value, and in particular is such that the gate-source voltage of the NMOS transistors 52, 54 of the current-to-voltage converter stage 18 is lower than the threshold voltage of the transistors themselves, the latter are off, and hence, when the equalization phase is terminated, no current is drained on the array branch 6. Consequently, the potentials of the output array node 56 and the output reference node 58 start to evolve as if the array memory cell 10 were written; i.e., the potential of the output array node 56 starts to increase, while the potential of the output reference node 58 starts to decrease.

[0026] If, however, the array memory cell 10 is erased, at a certain point the NMOS transistors 52, 54 of the current-to-voltage converter stage 18 turn on, and thus the potential of the output array node 56 stops increas-

ing and starts to decrease. When the potential of the output array node 56 is lower than the potential of the output reference node 58, the output signal OUT supplied by the comparator stage 19 then switches correctly to a high logic level.

[0027] If a too low equalization potential is chosen, the opposite problem is instead encountered. In fact, if the equalization potential to which the output array node 56 is brought during the equalization phase is lower than a preset reference value, in particular such that the gate-source voltage of the NMOS transistors 52, 54 of the current-to-voltage converter 18 is greater than the threshold voltage of the transistors themselves, the latter are overdriven, and the potentials of the output array node 56 and output reference node 58 then tend to evolve as if the array memory cell were erased; i.e., the potential of the output array node 56 starts to decrease at a rate faster than that at which the potential of the output reference node 58 decreases. Also contributing to this evolution is the array equivalent capacitor 76, which, in so far as it continues to drain current, simulates the presence of an erased cell.

[0028] If, however, the array memory cell 10 is written, at a certain point the potential of the output array node 56 stops decreasing and starts to increase. Also in this case, then, before a written array memory cell can be read, it is necessary to wait for the potential of the output array node 56 to reacquire the right value, with consequent dilation of the read time.

[0029] The problems of dilation of read times resulting from an incorrect definition of the equalization potential of the output array node 56 are moreover accentuated in the sense amplifier 1 described above by the fact that associated to the input array node 22 is the somewhat high (a few pF) capacitance of the array equivalent capacitor 76, and by the fact that, with the circuit structure of the sense amplifier 1 described above, in which it is the current drained by the array memory cell 10 that is mirrored on the reference branch 12, the current that flows in the array branch 6 is lower than the current that flows in the reference branch 12.

[0030] Figure 2 is a graphic representation of the consequences deriving from an incorrect definition of the equalization potential at a value higher than the above mentioned preset reference value for an erased array memory cell.

[0031] In particular, Figure 2 shows the plots versus time of the equalization signal SEQ and of the precharging signal SP, of the potentials V_M and V_R of the output array node 56 and of the output reference node 58 respectively, of the potential V_P of the input array node 22, and of the output signal OUT of the comparator stage 19 both during the equalization and precharging phases and during the read phase of an erased array memory cell.

[0032] During the equalization and precharging phases (in which the equalization signal SEQ and the precharging signal SP assume a high logic level), the potentials V_M and V_R, of the output array node 56 and of the output reference node 58 respectively, assume a value equal to the supply voltage V_{CC} decreased by a value equal to the threshold voltage of a PMOS transistor, the potential V_P of the input array node 22 assumes a value equal to 1 V, whilst the output signal OUT supplied by the comparator stage 19 assumes an intermediate value equal to approximately one half of that of the supply voltage V_{CC}.

[0033] Once the equalization and precharging phases are concluded (switching pulse edge of the equalization signal SEQ and of the precharging signal SP), the potential V_R of the output reference node 58 starts to decrease, whilst the potential V_M of the output array node 56 erroneously starts to increase. Consequently, the output signal OUT supplied by the comparator stage 19 and indicative of the binary information stored in the array memory cell 10 erroneously switches to a low logic level, which is indicative of a written memory cell.

[0034] During this anomalous initial transient, the input array node 22 is discharged by the current flowing in the array branch 6, and its potential V_P decreases slowly towards a value lower than 1 V; in particular, the potential V_P of the input array node 22 decreases by an amount such as to enable the regulator 48 to supply to the gate terminal of the NMOS transistor 44 a voltage increment sufficient for discharging the output array node 56.

[0035] When the potential V_P of the input array node 22 has dropped by a quantity that is sufficient for the NMOS transistor 44 to be able to discharge the output array node 56 and to bring the potential V_M of the said node to a value lower than the potential V_R of the output reference node 58, the output signal OUT supplied by the comparator stage 19 correctly switches to a high logic level indicative of an erased array memory cell.

[0036] From what has been described above, it is therefore evident that the time required for discharging the output array node 56, and hence for arriving at a correct reading of the binary information stored in the array memory cell 10, is markedly affected by the duration of the discharging transient of the input array node 22 by means of the current supplied by the array memory cell.

[0037] Given, however, that associated to the input array node 22 is a capacitance of a few pF of the array equivalent capacitor 76 and given that, with the circuit structure of the sense amplifier 1 described above (in which it is the current drained from the array memory cell 10 that is mirrored on the reference branch 12), the current flowing in the array branch 6 is not typically very high, and the duration of the discharging transient of the input array node 22 is relatively high, thus considerably limiting the reduction of read times at low supply voltages.

[0038] The aim of the present invention is therefore to provide a read circuit for a nonvolatile memory that is free from the drawbacks described above.

[0039] According to the present invention, a read circuit for a nonvolatile memory is therefore provided, as defined in Claim 1.

[0040] For a better understanding of the present invention, a preferred embodiment thereof will now be described, simply in order to provide a non-limiting example, with reference to the attached drawings, in which:

- Figure 1 shows a circuit diagram of a known sense amplifier;
- Figure 2 shows plots of electrical quantities of the sense amplifier of Figure 1 versus time;
- Figure 3 shows a circuit diagram of a sense amplifier according to the present invention; and
- Figure 4 shows plots of electrical quantities of the sense amplifier of Figure 3 versus time.

[0041] In Figure 3, the reference 1' designates, as a whole, a sense amplifier according to the present invention.

[0042] The sense amplifier 1' has a circuit structure largely similar to that of the sense amplifier 1 described previously, consequently the parts that are identical to those of the sense amplifier 1 will be designated by the same reference numbers, and differs from the latter in that it further comprises an array decoupling stage 80 arranged between the output array node 56 and the array biasing stage 40, and a reference decoupling stage 82 arranged between the output reference node 58 and the reference biasing stage 42, the said stages 80 and 82 having the purpose of rendering the potentials of the output array node 56 and the output reference node 58 independent of the potentials of the input array node 22 and, respectively, of the input reference node 32.

[0043] In particular, the array decoupling stage 80 and the reference decoupling stage 82 have identical circuit structures and each comprise first and second current mirrors 84, 86 and, respectively, 88, 90, cascaded between the drain terminal of the NMOS transistor 44, respectively 46, and the output array node 56, respectively the output reference node 58.

[0044] In detail, the first current mirrors 84 and 88 each comprise a first PMOS transistor 92 and a second PMOS transistor 94, respectively 96, 98, having gate terminals connected together and to the drain terminal of the PMOS transistor 92, respectively 96, and source and bulk terminals connected to the supply line 2. The PMOS transistors 92 and 96 moreover have drain terminals connected to the drain terminals of the NMOS transistor 44 and, respectively, of the NMOS transistor 46.

[0045] Each one of the first current mirrors 84 and 88 further comprises a third PMOS transistor 100, respectively 102, having gate terminal receiving a first enabling signal SN, respectively a second enabling signal ENM, source and bulk terminals connected to the supply line 2, and drain terminals connected to the gate terminals of the PMOS transistors 92, 94, respectively 96, 98.

[0046] The second current mirrors 86 and 90 each comprise a first NMOS transistor 104 and a second NMOS transistor 106, respectively 108, 110, having gate terminals connected together and to the drain terminal of the NMOS transistor 104, respectively 108, and defining a node 105, respectively 109, and source and bulk terminals connected to the ground line 4. The NMOS transistors 104 and 108 moreover have drain terminals connected to the drain terminals of the PMOS transistor 94 and, respectively, of the PMOS transistor 98, whilst the NMOS transistors 106 and 110 have drain terminals connected to the output array node 56 and, respectively, to the output reference node 58, bulk terminals connected to the ground line 4, and source terminals connected to the drain terminal of a transistor 112, which in turn has gate terminal receiving the first enabling signal SN and source and bulk terminals connected to the ground line 4.

[0047] Each one of the second current mirrors 84 and 88 further comprises a third NMOS transistor 114, respectively 116, having gate terminal receiving the first negated enabling signal $\overline{SN}$, respectively the second negated enabling signal $\overline{ENM}$, bulk and source terminals connected to the ground line 4 and drain terminal connected to the node 105, respectively 109.

The operation of the sense amplifier 1' will now be described solely as regards the array decoupling stage 80 and the reference decoupling stage 82, since the operation of the rest of the circuit is already known from the aforementioned European patent application.

[0048] In particular, the current mirrors 84 and 88 perform the function of decoupling the output array node 56 and the output reference node 58 from the input array node 22 and the input reference node 32 and, through the transistors 104 and 108, the current flowing in the array branch 6 is converted into a potential on the node 105, and the current flowing in the reference branch 12 is converted into a potential on the node 109.

[0049] The NMOS transistors 106, 110, connected in differential mode, thus carry out, jointly with the PMOS transistors 52, 54 which constitute their loads, the voltage comparison between the potentials of the nodes 105 and 109, and hence the output array node 56, which now is totally disengaged from the input array node 22 and from the capacitance associated thereto, can be quickly brought to a steady state value according to the voltage unbalancing between the nodes 105 and 109 themselves.

[0050] The PMOS transistors 100, 102 and the NMOS transistors 112, 114 and 116 perform secondary functions. In particular, the PMOS transistors 100 and 102 have the sole function of turning off the current mirrors 84 and 88 when the enabling signals SN and ENM assume a low logic level, the said current mirrors 84 and 88 consequently determining turning off of the current

mirrors 86 and 90, and thus considerable energy saving is achieved. The NMOS transistors 114 and 116, which are counterphase controlled with respect to the PMOS transistors 100 and 102, in that they receive, on their gate terminals, the negated enabling signals $\overline{SN}$, $\overline{ENM}$, have the function, when they are on, of bringing the nodes 105 and 109 back to the ground voltage V_{GND}; whilst the NMOS transistor 112, which is phase controlled together with the PMOS transistors 100, 102, in that it receives on gate terminal the enabling signal SN, has the function of turning off the current-to-voltage converter stage 18 and the transistors 106 and 110, which are connected in differential configuration, as well as the function of increasing the common mode rejection ratio (CMRR) of the transistors 106 and 110.

[0051] Figure 4 graphically highlights the advantage that the present invention makes possible as regards total reading time in the same operating conditions as those considered in Figure 2, i.e., in the case of an incorrect definition of the equalization potential at a value higher than the aforementioned preset reference value and in the case of an erased array memory cell.

[0052] In particular, Figure 4 is similar to Figure 2 and shows, with continuous lines, the plots versus time of the equalization signal SEQ, of the precharging signal SP, of the potentials V_M of the output array node 56 and V_R of the output reference node 58, of the potential V_P of the input array node 22, and of the output signal OUT of the comparator stage 19 for a sense amplifier according to the present invention, and, for comparison, with dashed lines, the plots versus time, already shown in Figure 2, of the potential V_M of the output array node 56 and of the potential V_P of the input array node 22 for a traditional sense amplifier.

[0053] As may be noted in this figure by comparing the continuous lines with the dashed lines, with the use of the circuit solution according to the present invention a reduction in the potential V_M of the output array node 56 is obtained that is decidedly faster than that obtained in a traditional sense amplifier. Consequently, in the sense amplifier according to the present invention, the instant in which the potentials V_M and V_R, of the output array node 56 and of the output reference node 58 respectively, intercross, and in which switching of the output signal OUT occurs, is clearly anticipated with respect to the case of a traditional sense amplifier, with consequent considerable reduction in total read time.

[0054] In addition, it may also be noted how the plot of the potential V_M of the output array node 56 is altogether uncorrelated with the plot of the potential V_P of the input array node 22, which even after termination of the equalization phase remains constant at 1 V.

[0055] A further advantage of the sense amplifier according to the present invention is that of enabling amplification as desired of the currents flowing in the array memory cell 10 and in the reference memory cell 16 through the mirror ratios of the transistors 94, 98, 106, and 110, thus enabling further reduction in the time required for discharging the output array node 56.

[0056] The advantages of the sense amplifier 1' according to the present invention are evident from what has been described previously.

[0057] Finally, it is clear that modifications and variations may be made to the sense amplifier 1' described and illustrated herein, without thereby departing from the sphere of protection of the present invention.

[0058] For example, in the sense amplifier 1', the diode connection present in the current-to-voltage converter stage 18 could also be made in a traditional way on the PMOS transistor 54 connected to the output reference node 58, instead of on the PMOS transistor 52 connected to the output array node 56, in order to be able to exploit the advantages of traditional current-to-voltage converters.

[0059] Furthermore, the circuit structure of the sense amplifier 1' could be simplified by eliminating the NMOS transistors 106, 110 and the PMOS transistors 52 and 54 of the current-to-voltage converter stage 18 and by connecting the comparator stage 19 directly to the nodes 105 and 109. According to this variant, then, the NMOS transistors 104 and 108 would perform the current-to-voltage conversion function, and the nodes 105 and 109 would consequently define the output array node and the output reference node, respectively.

[0060] This simplified structure could be further modified by connecting the NMOS transistors 104 and 108 together in such a way that they define a current mirror, i.e., by connecting the gate terminals of the NMOS transistors 104 and 108 together and by diode-connecting just one of these transistors, and then connecting the inverting terminal and the non-inverting terminal of the comparator stage 19 respectively to the drain terminal of the NMOS transistor 104 and to the drain terminal of the NMOS transistor 108.

[0061] Finally, the circuit structure of the sense amplifier 1' could be further simplified by eliminating also the reference decoupling stage 82, at the expense, however, of a loss of symmetry in the circuit structure itself.

Claims

1. A read circuit (1') for a nonvolatile memory cell, comprising a first reference line (2) and a second reference line (4) set, respectively, at a first reference potential (V_{CC}) and a second reference potential (V_{GND}) ; an array branch (6) having an input array node (22) connectable, via an array bit line (8), to an array memory cell (10) the contents of which it is desired to read; a reference branch (12) having an input reference node (32) connectable, via a reference bit line (14), to a reference memory cell (16) the contents of which are known; said array branch (6) and reference branch (12) further having an output array node (56; 105) and, respectively, an output reference node (58; 109); current-to-voltage

converter means (18; 104, 108) connected to said output array nodes (56; 105) and output reference nodes (58; 109) to supply, on the output array nodes (56; 105) and output reference nodes (58; 109), respective electric potentials (V_M, V_R) correlated to the currents flowing in said array memory cell (10) and, respectively, in said reference memory cell (16); and comparator means (19) connected at inputs to said output array nodes (56; 105) and output reference nodes (58; 109) and supplying at an output a signal (OUT) indicative of the contents stored in said array memory cell (10); characterized in that it further comprises array decoupling means (80) arranged between said input array node (22) and said output array node (56; 105) to decouple from one another the electric potentials of the input and output array nodes (22, 56; 22, 105).

2. The read circuit according to Claim 1, characterized in that said array decoupling means (80) comprise at least first current mirror means (84).

3. The read circuit according to Claim 2, characterized in that said first current mirror means (84) comprise a first transistor (92) and a second transistor (94) having first terminals connected to said input array node (22) and, respectively, to said output array node (105), and second terminals connected to said first reference line (2), and control terminals connected together and to the first terminal of said first transistor (92).

4. The read circuit according to Claim 3, characterized in that said array decoupling means (80) further comprise second current mirror means (86) arranged between said first current mirror means (84) and said output array node (56).

5. The read circuit according to Claim 4, characterized in that said second current mirror means (86) comprise a third transistor (104) and a fourth transistor (106) having first terminals connected to said first terminal of said second transistor (94) and, respectively, to said output array node (56), second terminals connected to said second reference line (4), and control terminals connected together and to the first terminal of said third transistor (104).

6. The read circuit according to any of the foregoing Claims, characterized in that it further comprises reference decoupling means (82) arranged between said input reference node (32) and said output reference node (58; 109) to decouple from one another the electric potentials of the input and output reference nodes (32, 58; 32, 109).

7. The read circuit according to Claim 6, characterized in that said reference decoupling means (82) comprise at least third current mirror means (88).

8. The read circuit according to Claim 7, characterized in that said current mirror means (88) comprise a fifth transistor (96) and a sixth transistor (98) having first terminals connected to said input reference node (32) and, respectively, to said output reference node (109), second terminals connected to said first reference line 2, and control terminals connected together and to the first terminal of said fifth transistor (96).

9. The read circuit according to Claim 8, characterized in that said reference decoupling means (82) further comprise fourth current mirror means (90) arranged between said third current mirror means (86) and said output reference node (58).

10. The read circuit according to Claim 9, characterized in that said fourth current mirror means (90) comprise a seventh transistor (108) and an eighth transistor (110) having first terminals connected to said first terminal of said sixth transistor (98) and, respectively, to said output reference node (58), second terminals connected to said second reference line (4), and control terminals connected together and to the first terminal of said seventh transistor (108).

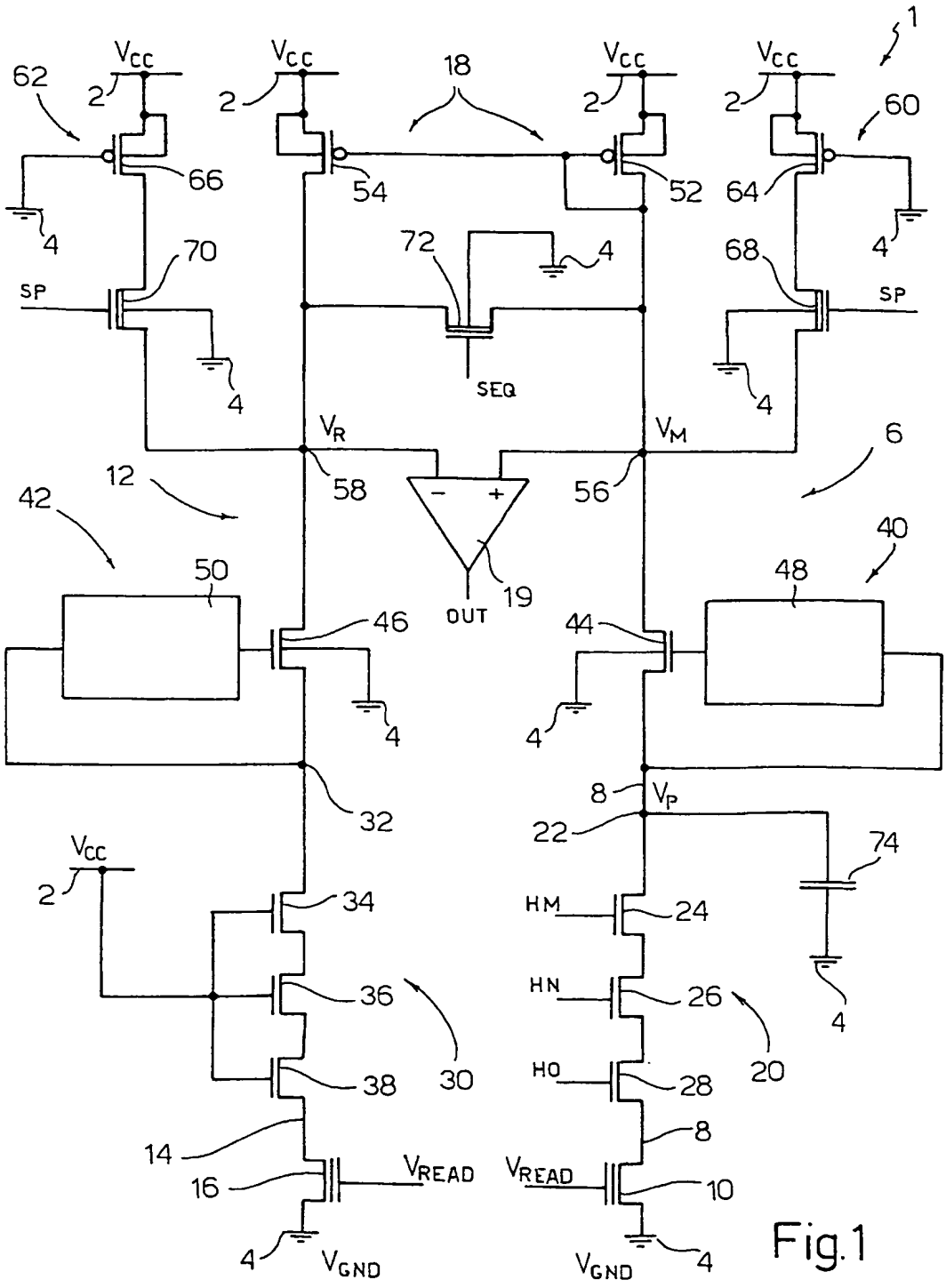
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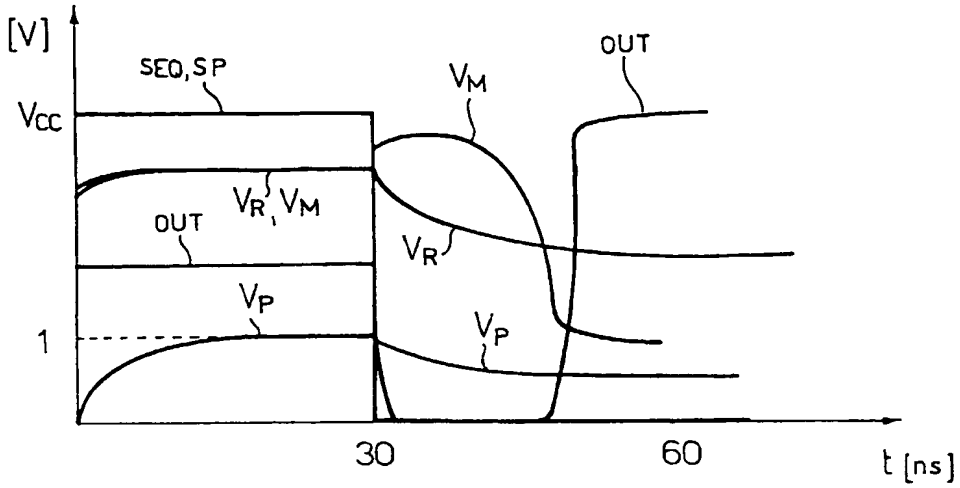
Fig.1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VM
OUT
VR, VM
OUT
VR
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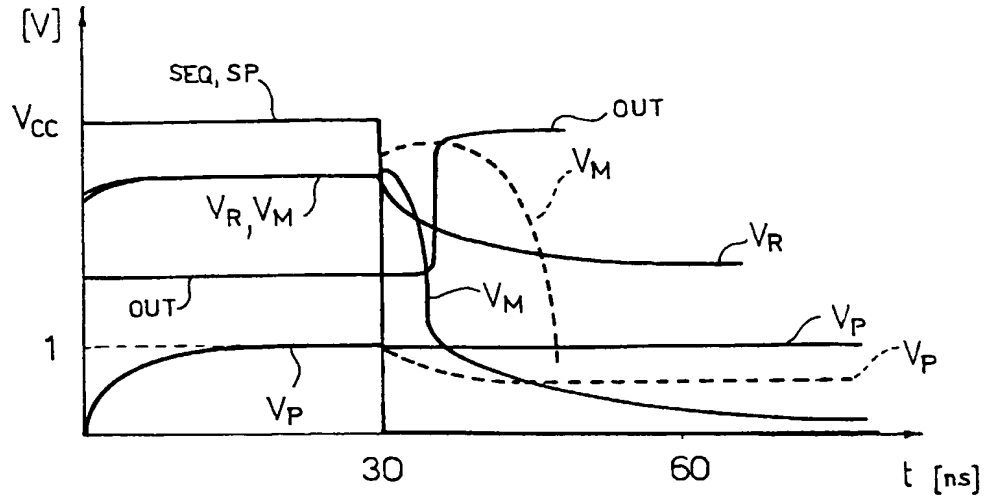
VP
1
30
60
t [ns]

Fig 2


[V]
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VR, VM
VR
OUT
VM
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VP
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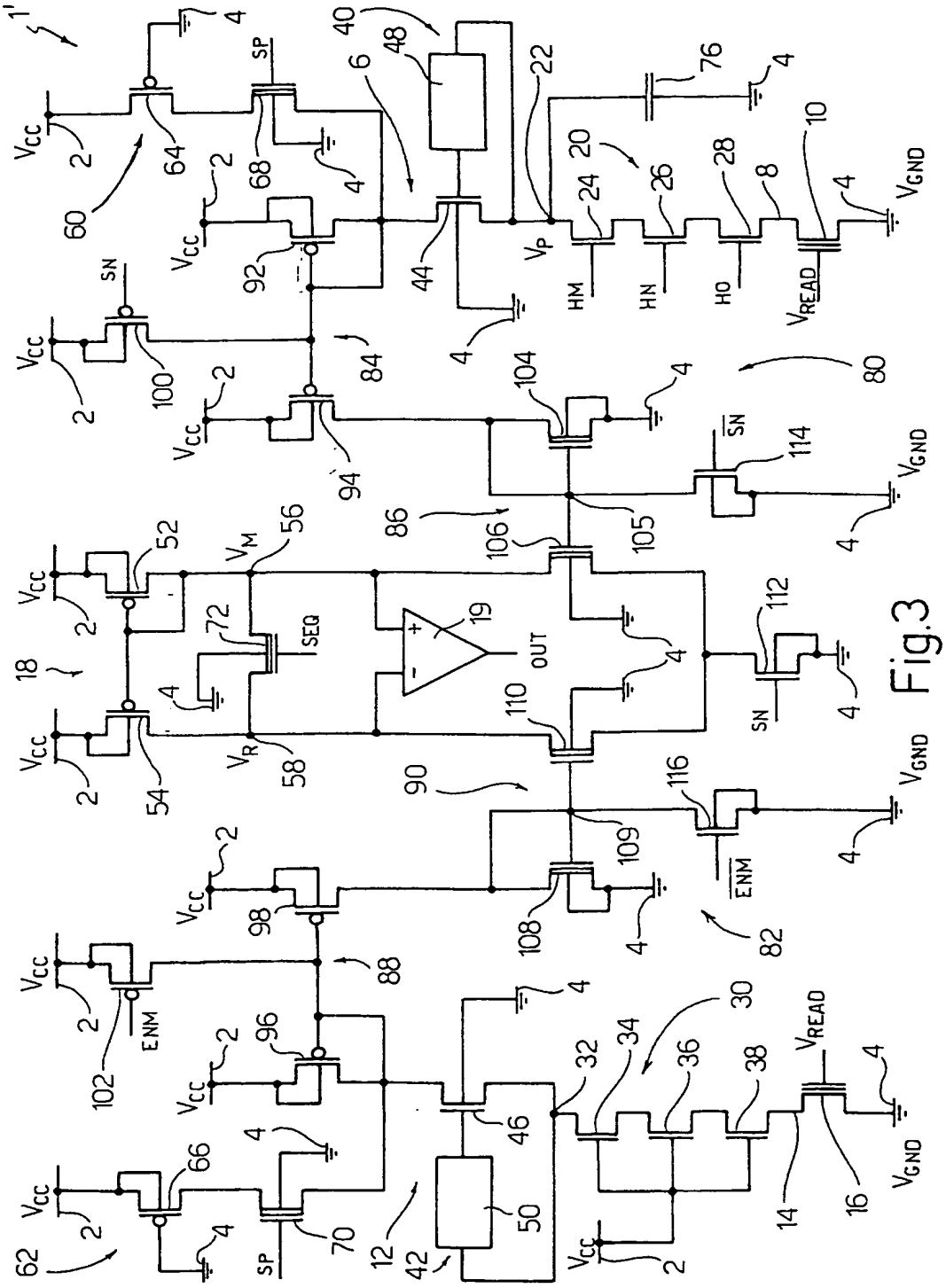
60
t [ns]

Fig.4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V_{GND}
V_P
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V_{READ}
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Fig.3

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EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0469

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Place of search	Date of completion of the search	Examiner
MUNICH	17 December 1999	Lindquist, J

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EPO FORM 1503 03.82 (P04C01)

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